Amendments to the Drawings

Please replace Figures 1 - 5 with Replacement Sheets containing revised Figures 1 -5 attached hereto.

REMARKS

I. Status of Claims

Claims 1-38 are pending.

Claims 1-38 stand rejected.

Claims 34 and 35 are amended herein.

II. Objections to the Specification

A.. Failure to Comply with 37 C.F.R. 184(p)(5), References in Figures Not Cited in Specification.

The examiner has noted a number of references in Figures 1 through 5 that are not cited in the text of the specification. The applicant has submitted new figures and made revisions to the specification consistent with the original disclosure. The following list details the resolution of the previously uncited references in Figures 1 through 5.

Drawing reference	Figure	Resolution
DQ0, DQ1, DQm, DQn, DQz	1,2, 3	References deleted
COL 0, COL n, COL R	3	References deleted
451a ... 451z	3	Citation added to ¶45
265a ... 265z	3	Citation added to ¶45
WRTIE from n1, READ n+1, READ n, WRITE n, WRITE to n+1	4	Citation added to ¶45, drawing corrected to indicate "WRITE from n1"
459	4	Citation appeared in

		original ¶45 line 14, no change required, additional references added for clarification
neihit	4	Citation modified in ¶46 to refer to "neihit"
iohit	4	Citation added to ¶45
DQx	4	Citation added to ¶45
iohit 0L, iohit 1L, iohit 2L, iohit nL, iohit 0R, iohit 1R, iohit 2R, iohit nR	5	Citation added to ¶46
neihit 0, neihit 1, neihit 2, neihit m	5	Citation added to ¶51
neihit n, neihit n+1, neihit n+2, neihit n	5	References deleted
MUX CTRL a, MUX CTRL b, MUX CTRL c, MUX CTRL m, MUX CTRL z, MUX CTRL y, MUX CTRL x, MUX CTRL n	5	Citation added to ¶48
415a	5	Citation appeared in original ¶48 line 4.
430a, 430b, 430m	5	Citation appeared in original ¶51
430c	5	Citation implied in original ¶51 "430b, ... 430m." Paragraph 51 revised to specifically cite "430c."
430n, 430x, 430y, 430z	5	Citation added to ¶51
MUX REDUN, L/R, SW, 407z	5	References deleted
FUSE 0, FUSE 1, FUSE 2 and FUSE m	5	References deleted

B. Failure to Comply with 37 C.F.R. 184(p)(5), References in Description not Shown in Drawings.

The examiner has noted a number of references in the description that do not appear in any of the figures. The applicant has submitted new figures and made revisions to the specification consistent with the original disclosure. The following list details the resolution of the missing references.

Description reference	Resolution
225a ... 225z	Reference added to Fig. 3 in area marked "SUB ARRAY 0"
230a, 230b ... 230z	Reference added to Fig. 3 in area marked "Sub Array 0"
260a, 260m, 260n and 260z	Citations deleted.
(iohitnx) 405	Citation revised to 405b, which appears in Fig. 5 at upper left.
235 of memory cells 240a, 240b and 240z	Reference appears in original Fig. 3 at upper right center.
(neihit a) 430a	Citation revised to (neihit 0) 430a, which appears in Fig. 5.
300a, 295a	Citations changed to 300, 295 which appear in Fig. 4.
(neihit x) 430b ... 430m	Revised citation to neihit 1, which appears in Fig. 5 at upper left quarter.
300b ... 300m	Citation revised to 300, which appears in Fig. 4.
295b ... 295m	Citation revised to 295, which appears in Fig. 4.
295m	Citation revised to 295, which appears in Fig. 4.
305	Reference appears in original Fig. 3 at lower center right.
260m	Citation revised to 260, which appears in Fig. 4.
260n ... 260z	Citation revised to 260, which appears in Fig. 4.

III. Claim Rejections Under 35 U.S.C. § 112

The examiner has rejected claims 1-38 as "failing to comply with the enablement requirement." In particular, the examiner has cited the missing drawing references and citations which the applicant has addressed and corrected herein.

Additionally, the examiner has requested that the applicant "point out each of recited elements in claims 1-38 to be read on which element in the drawings of the present invention. Without limiting the claims to the embodiments described in the specification, applicant responds as follows, with references to figures pointing out elements in bold. Only independent claims and those listing additional elements that can be pointed to in the figures are listed.

1. A yield enhancement circuit for substituting a redundant circuit for a faulty circuit of an integrated circuit, comprising:

a plurality of fault indication devices **[e.g. OR gate 256, Fig. 5]**, wherein each fault indication device is associated with one sub-circuit **[e.g. SUB ARRAY 0, 215a Fig. 3]** of the integrated circuit such that one fault indication device is activated to generate a fault signal **[e.g. 410b Fig. 5]** to express existence of a fault within the faulty circuit of said integrated circuit, additionally each fault indication device that is associated with selected adjacent sub-circuits **[e.g. the OR gate in block 250c, Fig 5]** of the integrated circuit activates the fault signal to express existence of the fault within the faulty circuit of said integrated circuit;

a fault detection device **[e.g. "Y-Fuse" 280, Fig. 5]** in communication with the plurality of fault indication devices to determine the existence of the faulty circuit within the integrated circuit and transmit a redundancy implementation signal **[e.g. 415a, 415b, Fig. 3]** upon determination of existence of the faulty circuit; and

a plurality of redundancy activation circuits **[e.g. MUX I/O circuits 450a ... 450m, Fig. 3]** in communication with the fault detection device to receive the redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the sub-circuit to which said fault indication device is associated and to which said fault indication device selectively transfers input/output signals **[e.g. reads and writes via 265a, Fig. 3]** of the sub- circuit associated with the fault indication device **[e.g. 215a, Fig. 3]** and its adjacent sub-circuit **[e.g. 215b, Fig. 3]** to a designated path dependent on the expression of the existence of a fault within the integrated circuit.

7. The yield enhancement circuit of claim 5 wherein each of the sub-circuits comprises a column of memory cells **[e.g. 225a, Fig. 3]** and a read/write buffer **[e.g. 255a, Fig 3]** connected to the column of memory cells.

8. The yield enhancement circuit of claim 1 wherein the designated path is an input/output driver/receiver circuit **[e.g. 260, Fig. 4]** that transfers the input/output signals from/to external circuitry.

9. The yield enhancement circuit of claim 1 wherein each fault indication device comprises a fuse, **[252 (F1), Fig 5]** whereby when said fuse is intact, said sub-circuit does not contain the fault and when said fuse is not intact, said sub-circuit contains the fault.

10. The yield enhancement circuit of claim 9 wherein each fault indication device further comprises a logical combining circuit **[256, Fig. 5]** to logically combine each fault

signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent sub-circuits.

11. A yield enhancement circuit within a memory integrated circuit for substituting redundant groups of memory cells for faulty groups of memory cells within said memory integrated circuit, comprising:

a plurality of fault indication devices **[e.g. OR gate 256, Fig. 5]**, wherein each fault indication device is associated with one group of memory cells **[e.g. SUB ARRAY 0, 215a Fig. 3]** of the memory integrated circuit such that one fault indication device is activated to generate a fault signal **[e.g. 410b, Fig. 5]** to express existence of a fault within the faulty group of memory cells of said memory integrated circuit, additionally each fault indication device that is associated with a selected adjacent group of memory cells **[e.g. the OR gate in block 250c, Fig. 5]** of the memory integrated circuit generates the fault signal **[e.g. 410c, Fig. 5]** to express the existence of the fault within the faulty group of memory cells of said memory integrated circuit;

a fault detection device **["Y-Fuse" 280, Fig. 3]** in communication with the plurality of fault indication devices to determine the existence of the faulty group of memory cells within the memory integrated circuit and transmit a redundancy implementation signal **[e.g. 415a, 415b, Fig. 3]** upon determination of existence of the faulty group of memory cells; and

a plurality of redundancy activation circuits **[e.g. MUX I/O circuits 450a ... 450m, Fig. 3]** in communication with the fault detection device to receive the

redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the group of memory cells to which said fault indication device is associated and associated to an adjacent group of memory cells of said group of memory cells to which said fault indication device is associated to selectively transfer input/output signals **[e.g. reads and writes via 265a, Fig. 3]** of the group of memory cells associated with the fault indication device **[e.g. 215a, Fig. 3]** and its adjacent group of memory cells **[e.g. 215b, Fig. 3]** to a designated path dependent on the expression of the existence of a fault within the memory integrated circuit.

16. The yield enhancement circuit of claim 15 wherein each of the group of memory cells comprises a column of memory cells **[e.g. 225a, Fig. 3]** and a read/write buffer **[e.g. 255a, Fig. 3]** connected to the column of memory cells to selectively sense data stored in said column of memory cells and to store data to said column of memory cells.

17. The yield enhancement circuit of claim 11 wherein the designated path is an input/output driver/receiver circuit **[e.g. 260, Fig. 4]** that transfers the input/output signals from/to external circuitry.

18. The yield enhancement circuit of claim 11 wherein each fault indication device comprises a fuse, **[e.g. 252 (F1), Fig. 5]** whereby when said fuse is intact, said group of memory cells does not contain the fault and when said fuse is not intact, said group of memory cells contains the fault.

19. The yield enhancement circuit of claim 18 wherein each fault indication device further comprises a logical combining circuit **[e.g. 256, Fig. 5]** to logically combine each fault signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent group of memory cells.

20. A memory comprising:

at least one array of memory cells, **[e.g. 215a, Fig. 5]** each array of memory cells arranged in rows and columns of memory cells;

at least one redundant column of memory cells **[e.g. 235, Fig. 5]** associated with at least one of said arrays of memory cells to replace a faulty column of memory cells; and

a yield enhancement circuit in communication with at least one array of said memory cells and said redundant columns of memory cells for substituting redundant column of memory cells for a faulty column of memory cells within said associated arrays of memory cells, said yield enhancement circuit comprising:

a plurality of fault indication devices, **[e.g. OR gate 256, Fig. 5]** wherein each fault indication device is associated with one column of memory cells **[e.g. 225a, Fig. 3]** of the arrays of memory cells such that one fault indication device is activated to generate a fault signal **[e.g. 410b, Fig. 5]** to express existence of a fault within the faulty column of memory cells of said arrays memory cells, additionally each fault indication device that is associated with a selected adjacent column of memory cells of the arrays of memory cells **[e.g. the OR gate in block 250c, Fig. 3]** generates the fault signal to

express existence of the fault within the faulty column of memory cells of said arrays of memory cells;

a fault detection device **["Y-Fuse" 280, Fig. 3]** in communication with the plurality of fault indication devices to determine the existence of the faulty column of memory cells within the arrays of memory cells and transmit a redundancy implementation signal **[e.g. 415a, 415b, Fig. 3]** upon determination of existence of the faulty column of memory cells; and

a plurality of redundancy activation circuits **[e.g. MUX I/O circuits 450a ... 450m, Fig. 3]** in communication with the fault detection device to receive the redundancy implementation signal, each redundancy activation circuit in communication with one of the fault indication devices and associated with the column of memory cells **[e.g. 225a, Fig. 3]** to which said fault indication device is associated and associated to an adjacent column of memory cells **[not illustrated in Fig. 3 is the next adjacent column of memory cells to 225a, but such a column would be 225b. See description at ¶ 44 explaining redundancy circuit could be connected by single column or multiple columns]** of said column of memory cells to which said fault indication device is associated to selectively transfer input/output signals **[e.g. reads and writes via 265a, Fig. 3]** of the column of memory cells associated with the fault indication device **[e.g. 225a]** and its adjacent column of memory cells to a designated path dependent on the expression of the existence of a fault within the arrays of memory cells.

25. The memory of claim 24 wherein each of the column of memory cells comprises a column of memory cells **[e.g. 225a, Fig. 3]** and a read/write buffer **[e.g. 255a, Fig. 3]** connected to the column of memory cells to selectively sense data stored in selected memory cells and to store data to said selected memory cells.

26. The memory of claim 20 wherein the designated path is an input/output driver/receiver circuit **[e.g. 260, Fig. 4]** that transfers the input/output signals from/to external circuitry.

27. The memory of claim 20 wherein each fault indication device comprises a fuse, **[e.g. 252 (F1), Fig. 5]** whereby when said fuse is intact, said column of memory cells does not contain the fault and when said fuse is not intact, said column of memory cells contains the fault.

28. The memory of claim 27 wherein each fault indication device further comprises a logical combining circuit **[e.g. 256, Fig. 5]** that logically combine each fault signal of each fault indication device with the fault signal of the fault indication device that is associated with selected adjacent column of memory cells.

29. A method for yield enhancement of an integrated circuit by substituting a redundant circuit for a faulty circuit of said integrated circuit, comprising the steps of:

providing fault indication **[e.g. 405b. Fig. 5]** associated with each sub-circuit of the integrated circuit such that one fault indication generates a fault signal **[e.g. 410b. Fig. 5]** to express the existence of a fault within the faulty circuit of said integrated circuit, additionally each fault indication associated with selected adjacent sub-circuits

[e.g. 405c, Fig. 5] of the integrated circuit generates the fault signal to express the existence of the fault within the faulty circuit of said integrated circuit;

determining the existence of the faulty circuit within the integrated circuit from said fault signal;

generating a redundancy implementation signal **[e.g. 415a, Fig. 3]** upon determination of existence of the faulty circuit; and

initiating redundancy activation **[e.g. via MUX I/O circuits 450a ... 450m, Fig. 3]** upon generating the redundancy implementation signal and one of the fault indications associated with the sub-circuit to selectively transfer input/output signals **[e.g. reads and writes via 265a, Fig. 3]** of the sub- circuit associated with the fault indication **[e.g. 215a, Fig. 3]** and an adjacent sub-circuit **[e.g 215b]** to a designated path dependent on the expression of the existence of a fault within the integrated circuit.

35. The method of claim 34 wherein each of the sub-circuits comprise a column of memory cells **[e.g. 225a, Fig. 3]** and a read/write buffer **[e.g. 255a, Fig. 3]** connected to the column of memory cells.

36. The method of claim 29 wherein the designated path is an input/output driver/receiver circuit **[e.g. 260, Fig. 4]** that transfers the input/output signals from/to external circuitry.

37. The method of claim 29 wherein each fault indication is generated by a fuse, **[e.g. 252 (F1), Fig. 5]** whereby when said fuse is intact, said sub-circuit does not contain the fault and when said fuse is not intact, said sub-circuit contains the fault.

38. The method of claim 37 wherein each fault indication further generates a logical combining circuit **[e.g. 256, Fig. 5]** that logically combines each fault indication with the fault indication that is associated with selected adjacent sub-circuits.

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

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